

A perspective view of a semiconductor device 100. The device includes a substrate 110 with a stack of layers 111, 112, 113, 114, 115, and 116. A gate stack 120 is formed on the substrate, comprising layers 121, 122, 123, 124, 125, and 126. A source/drain region 130 is formed on the substrate, comprising layers 131, 132, 133, 134, and 135. A dashed line II-II indicates a cross-section through the device.

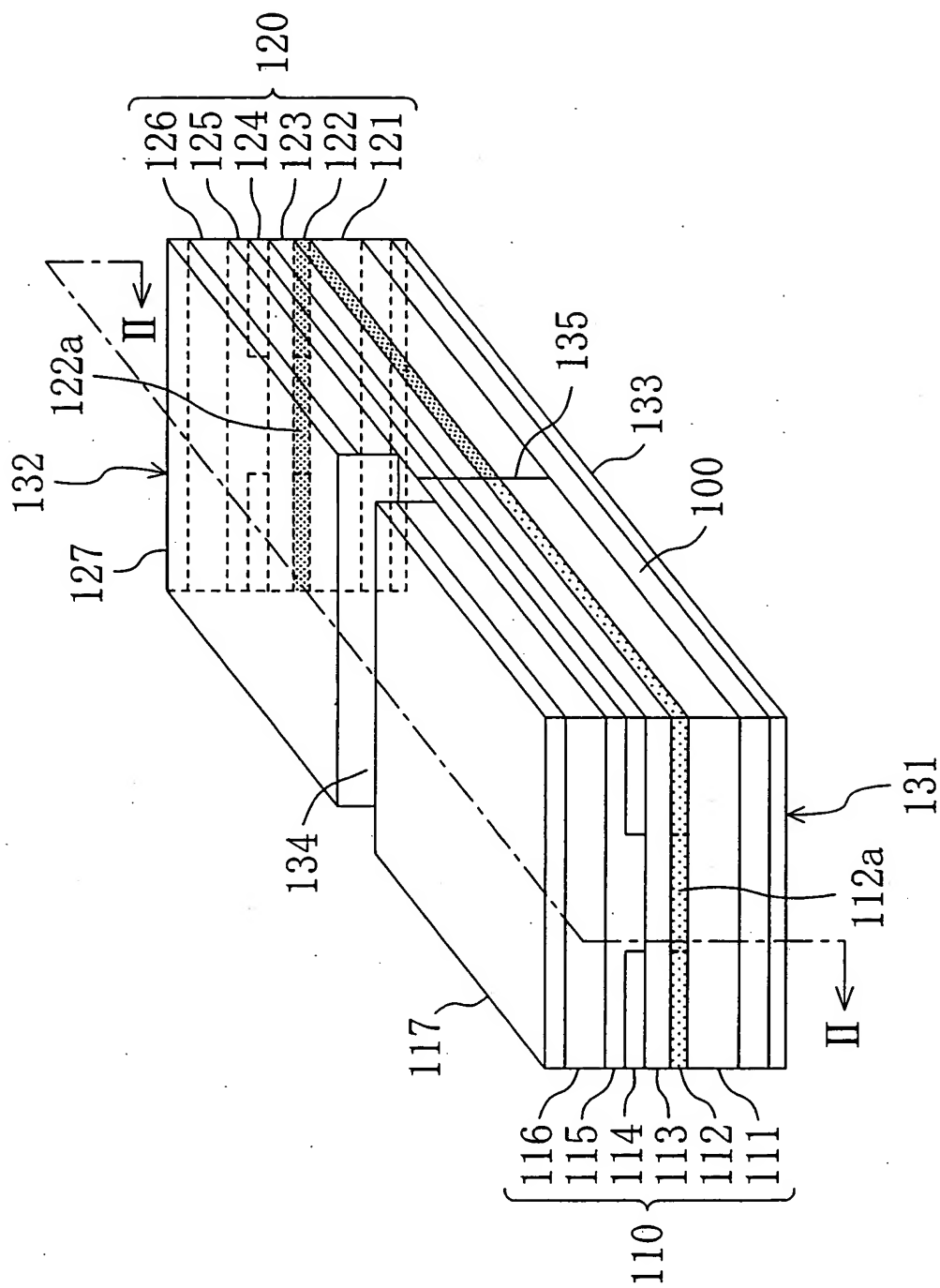


FIG. 2

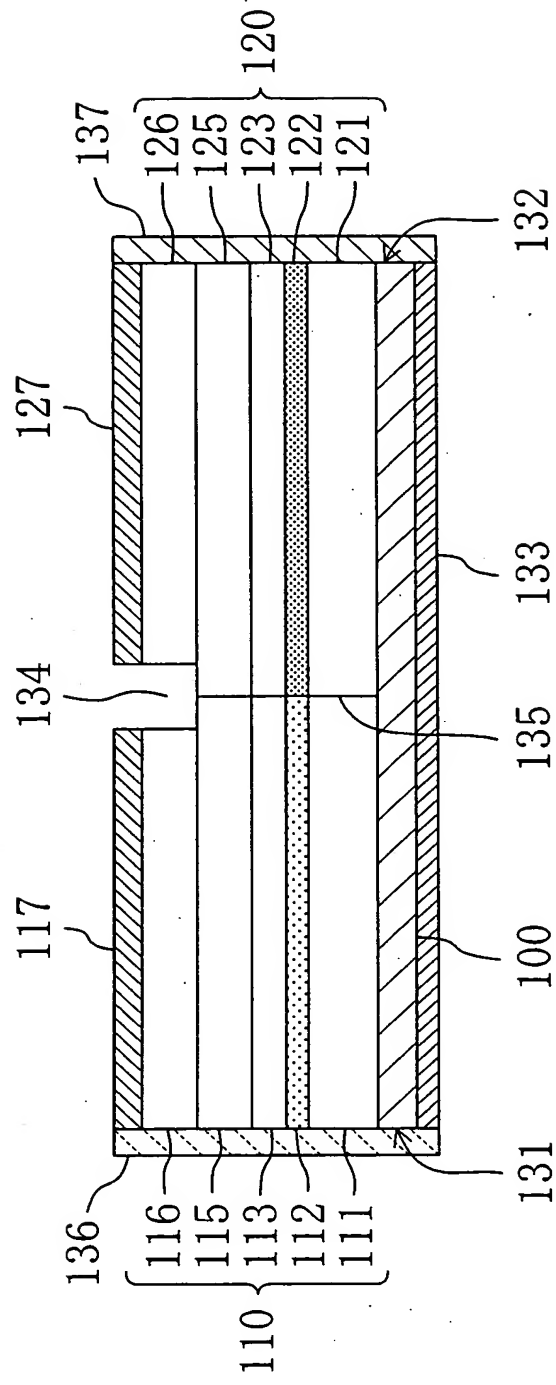


FIG. 3

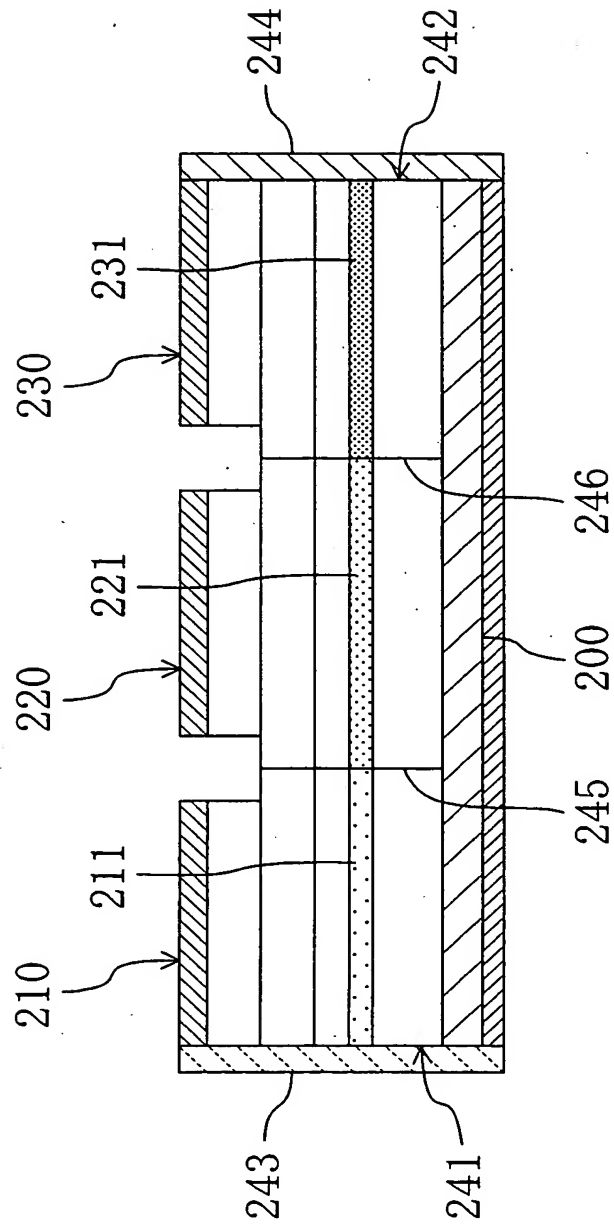


FIG. 6A

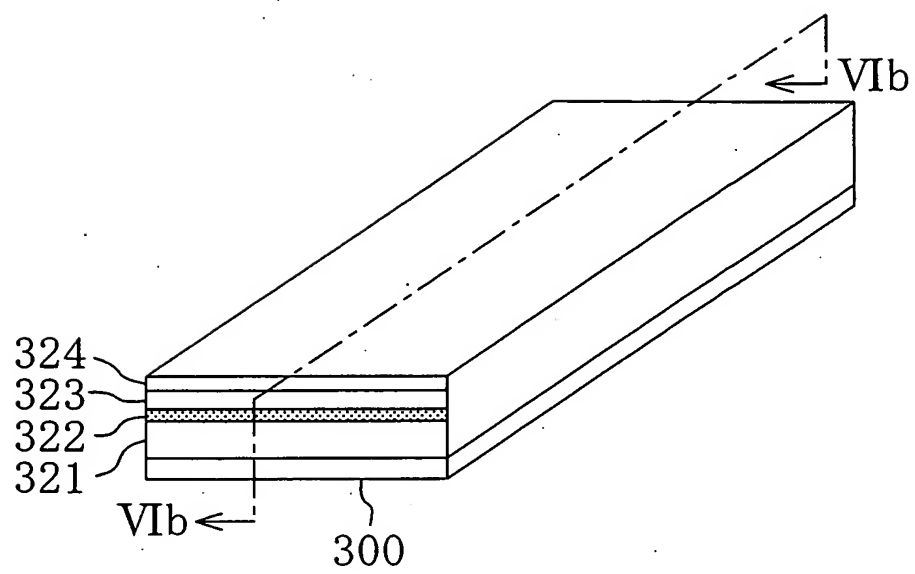


FIG. 6B

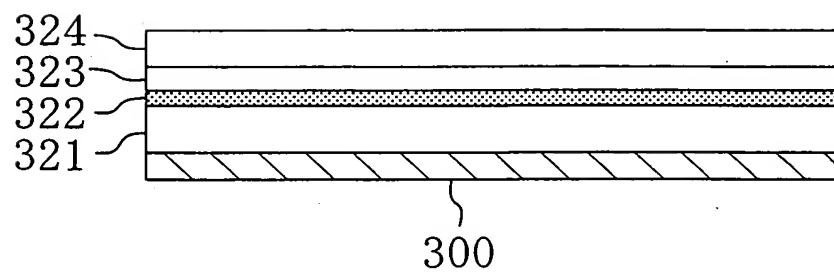


FIG. 7A

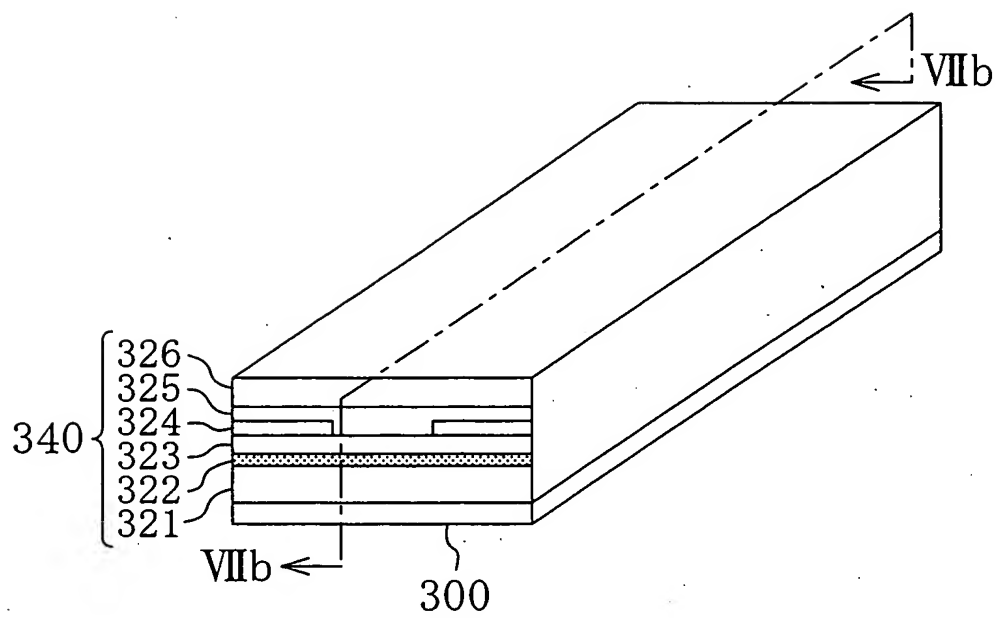


FIG. 7B

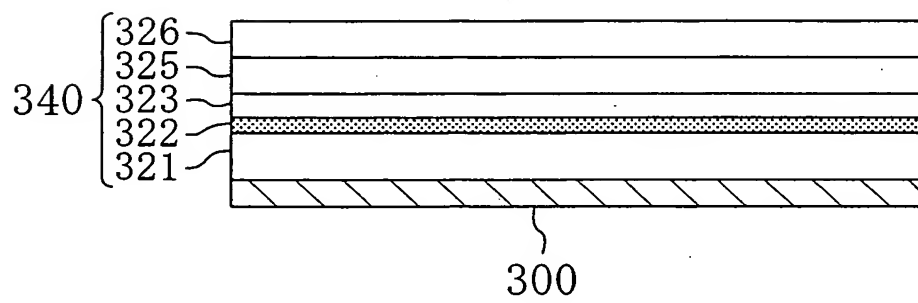


FIG. 8A

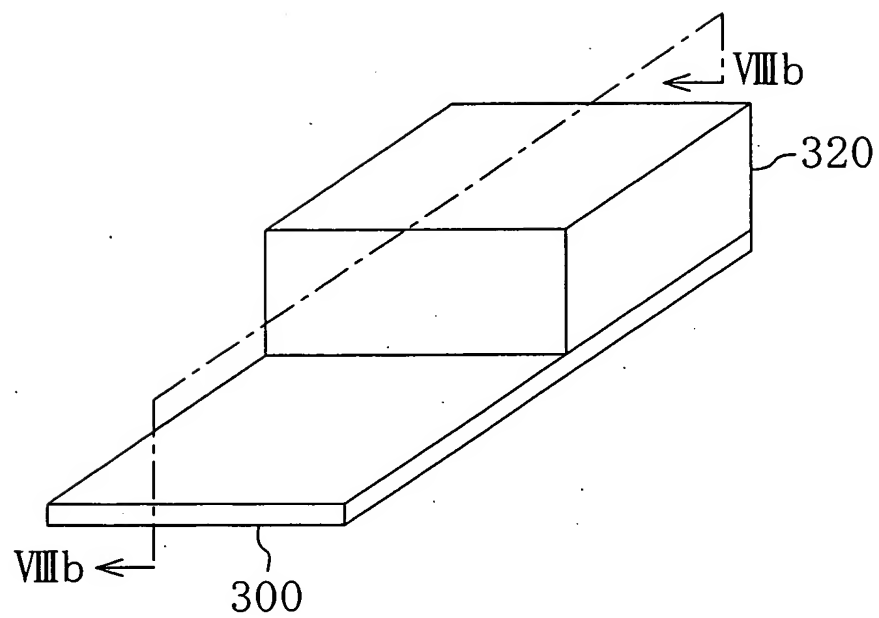


FIG. 8B

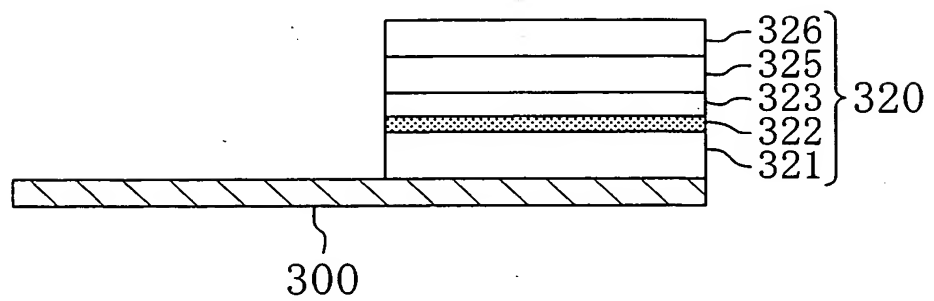


FIG. 9A

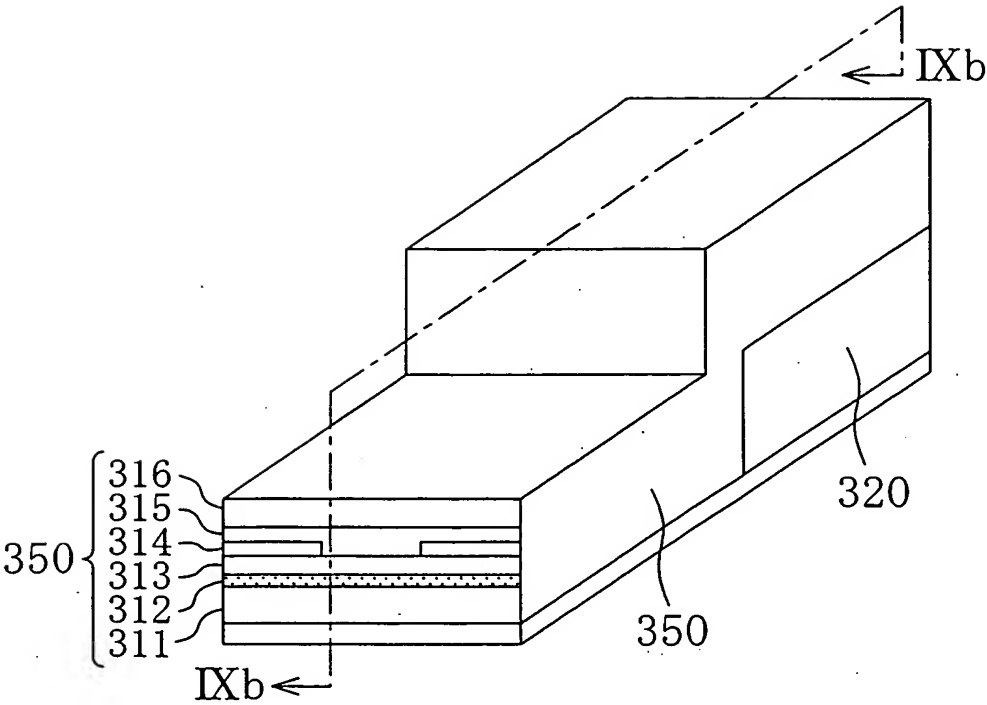


FIG. 9B

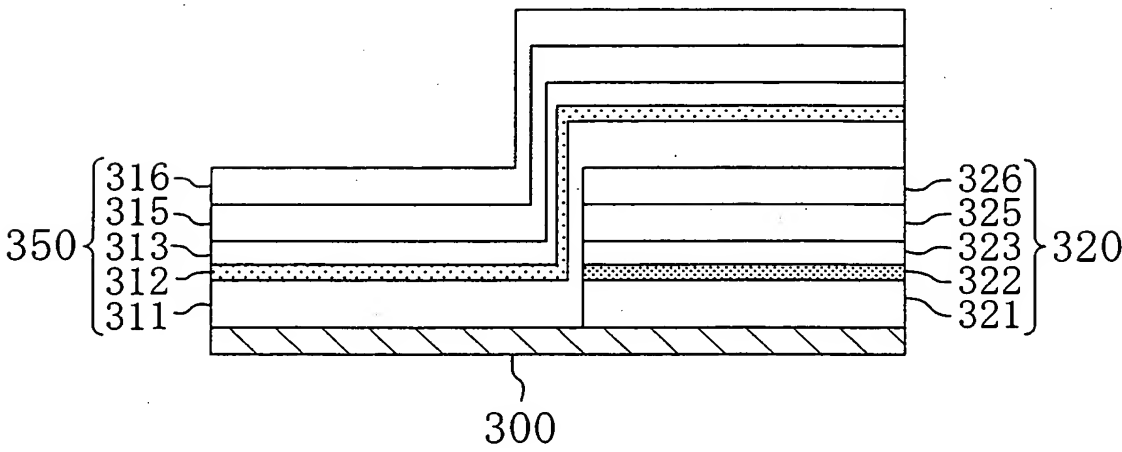


FIG. 10A

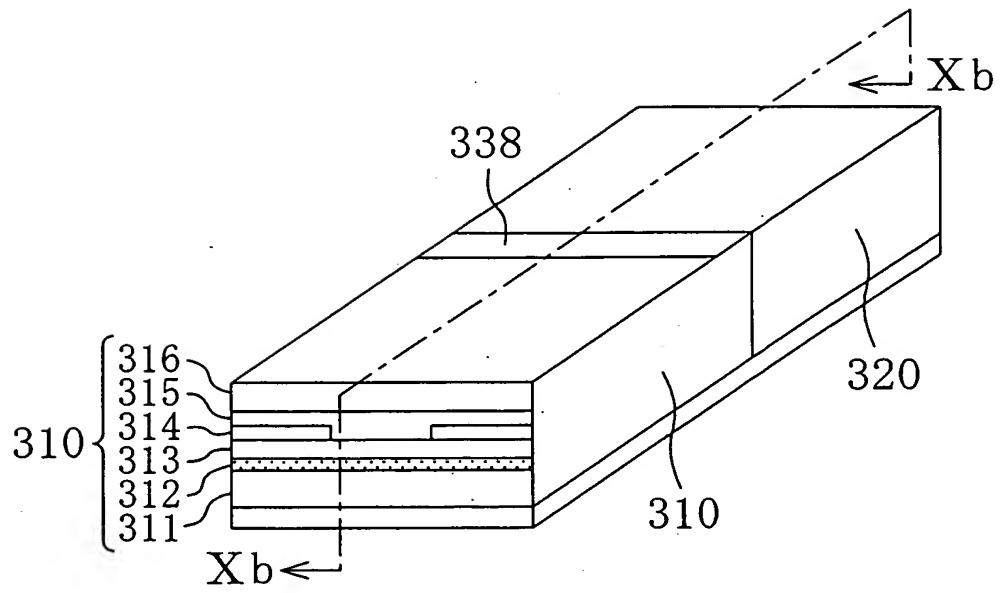


FIG. 10B

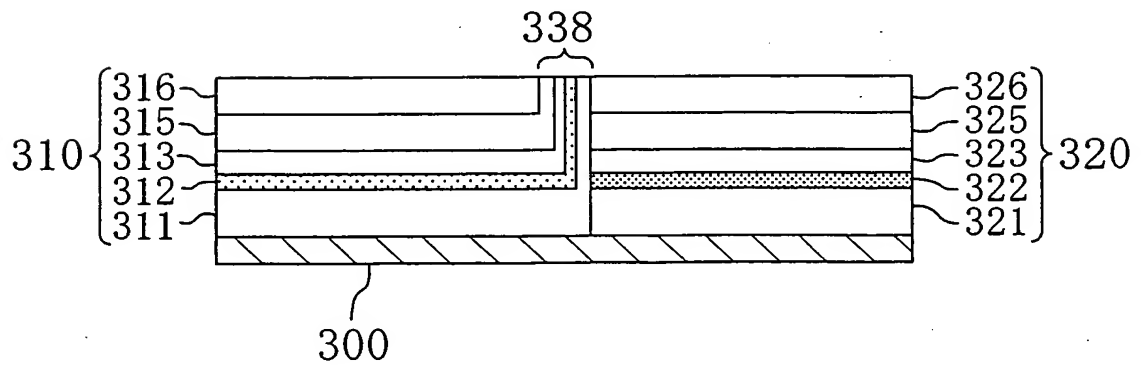


FIG. 11A

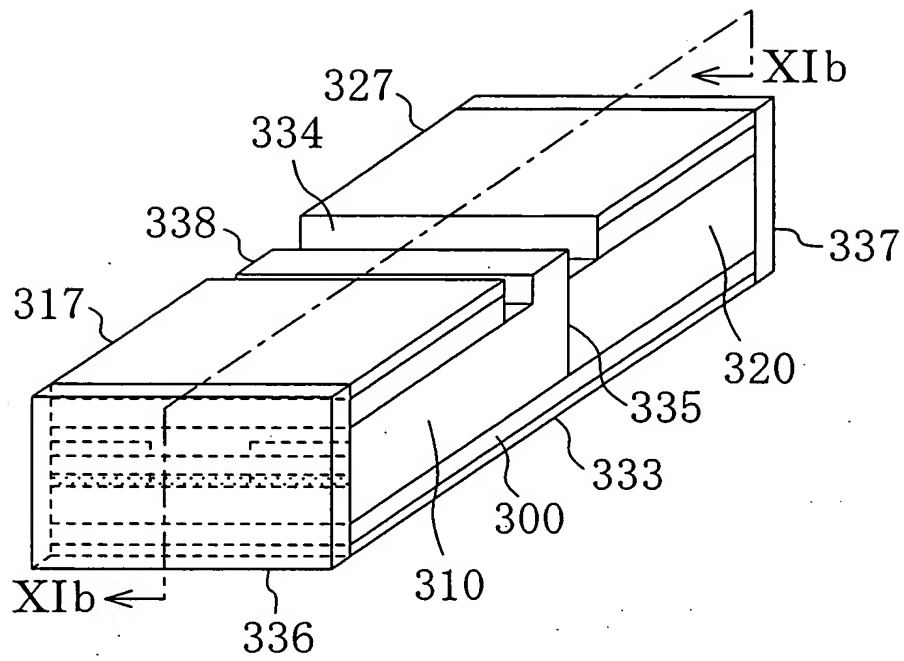


FIG. 11B

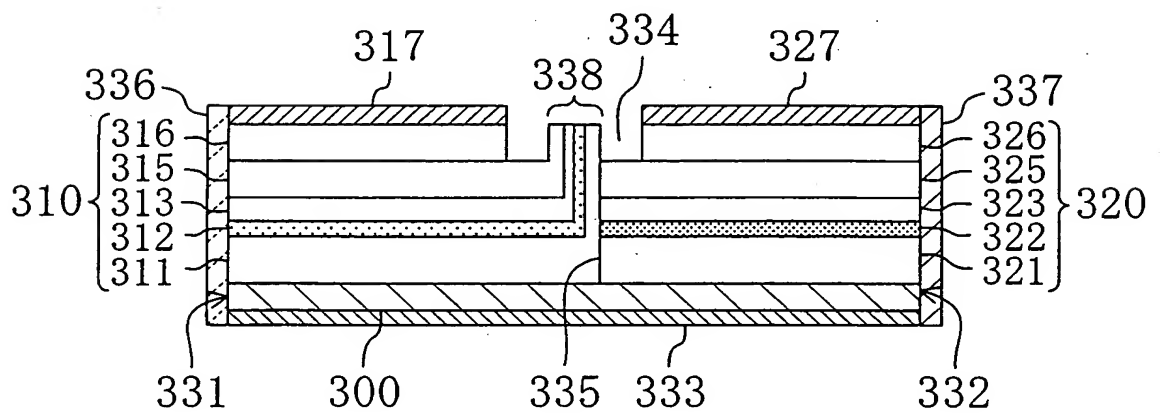


FIG. 12

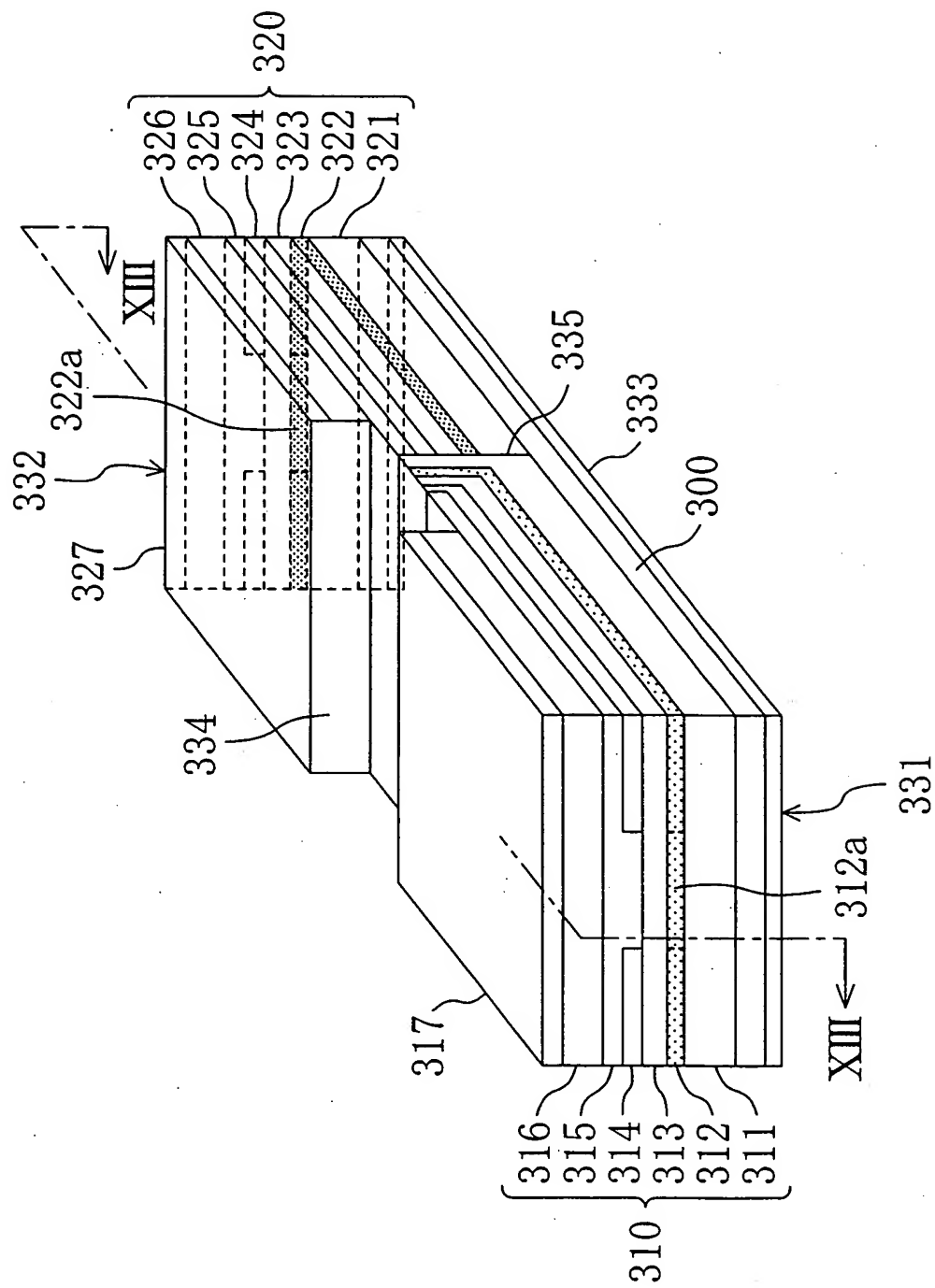


FIG. 13

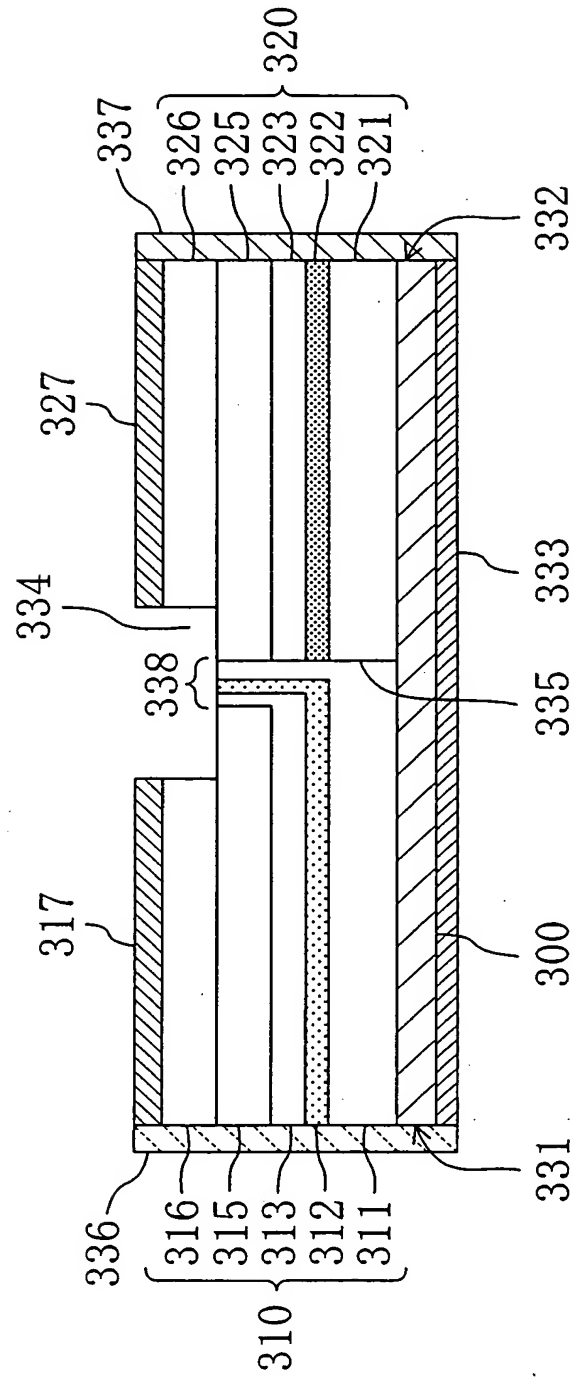


FIG. 14A

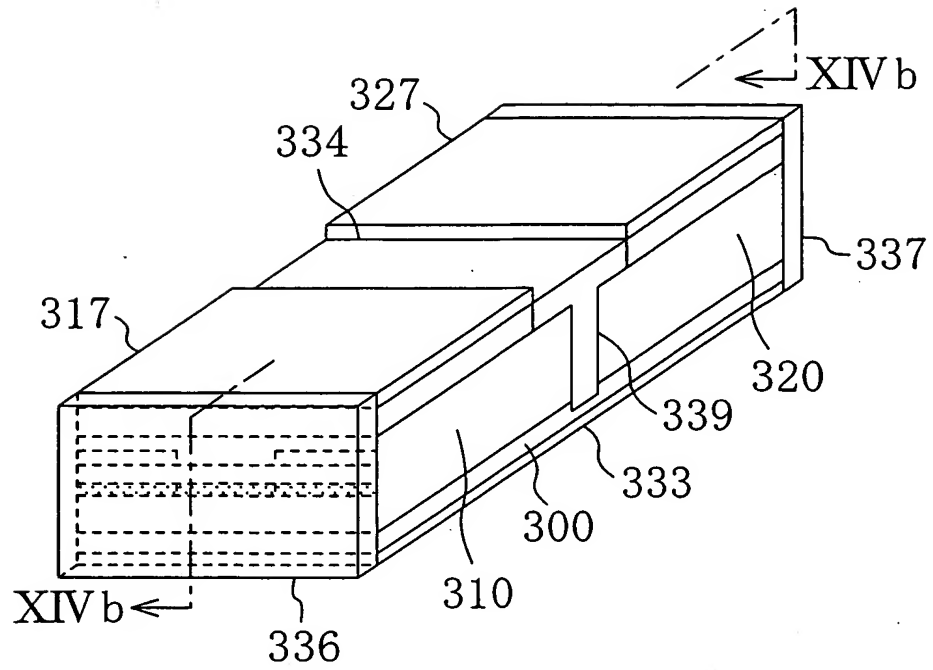


FIG. 14B

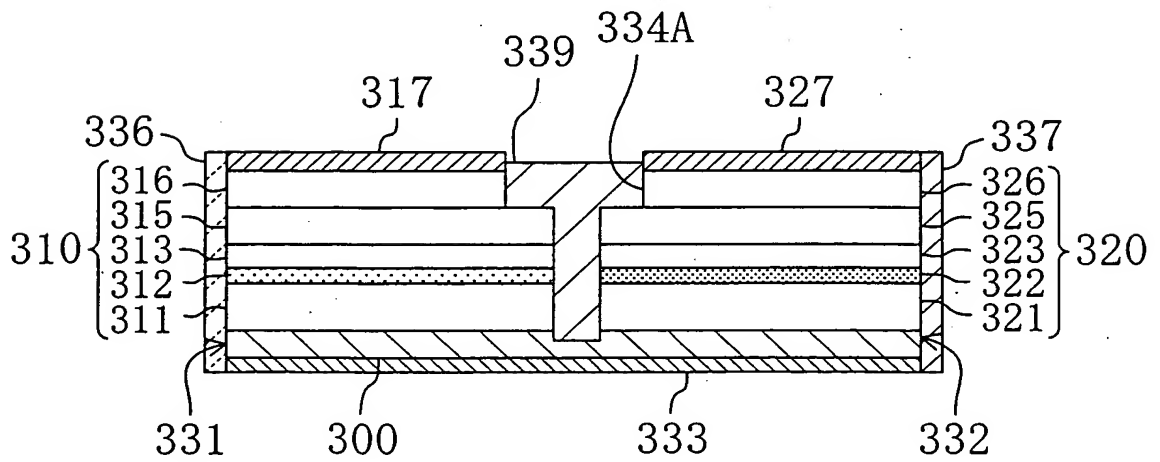


FIG. 16A

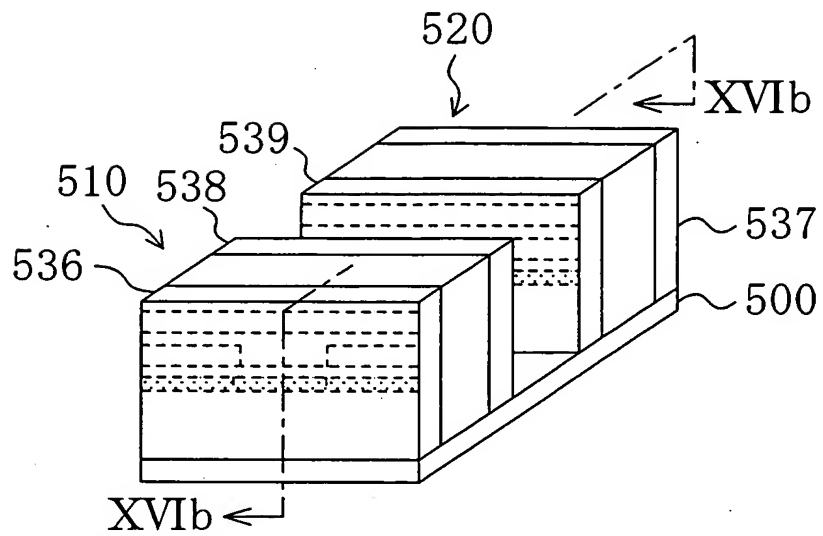


FIG. 16B

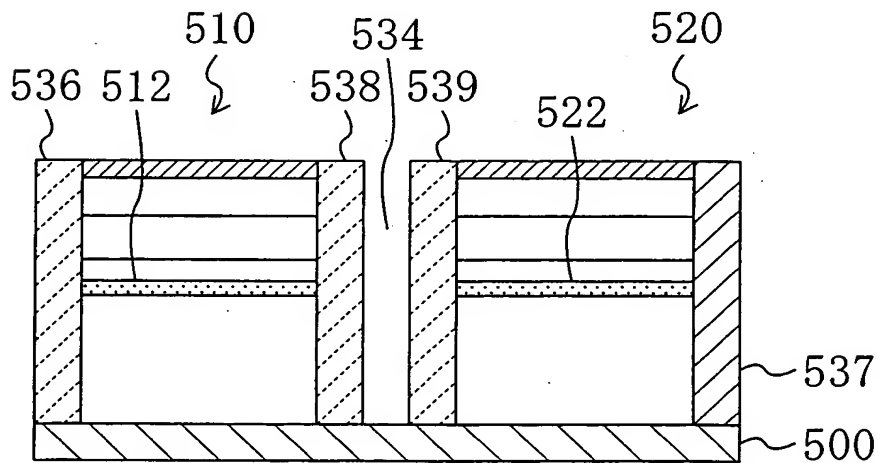


FIG. 17

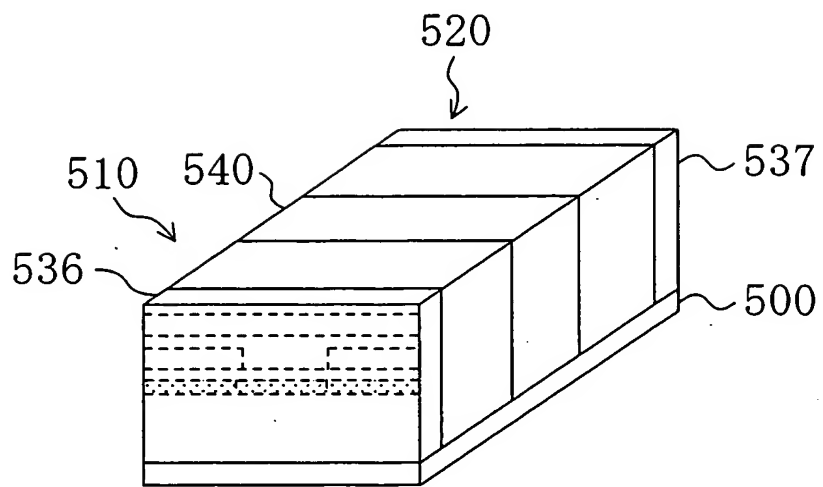


FIG. 18

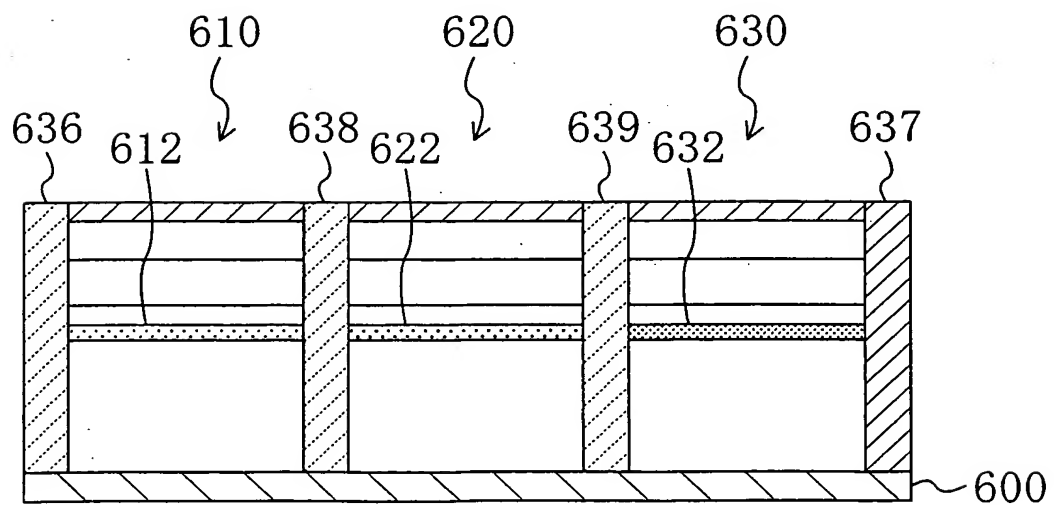


FIG. 19A

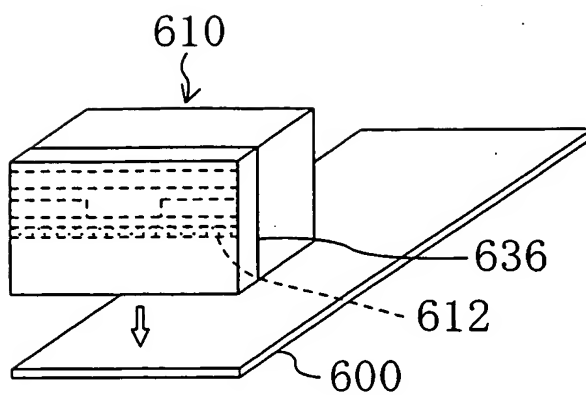


FIG. 19B

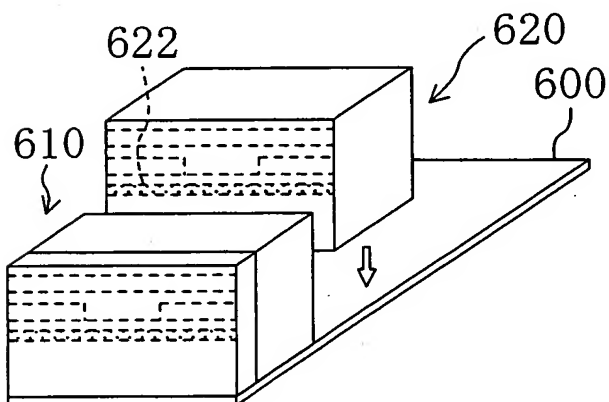


FIG. 19C

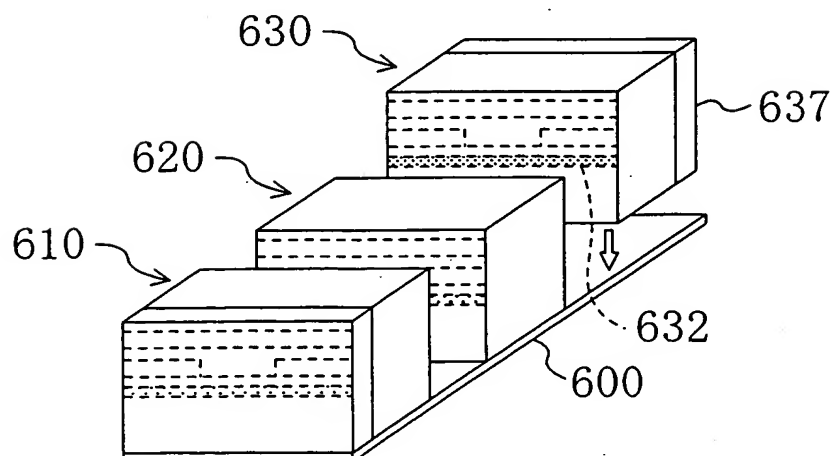


FIG. 20

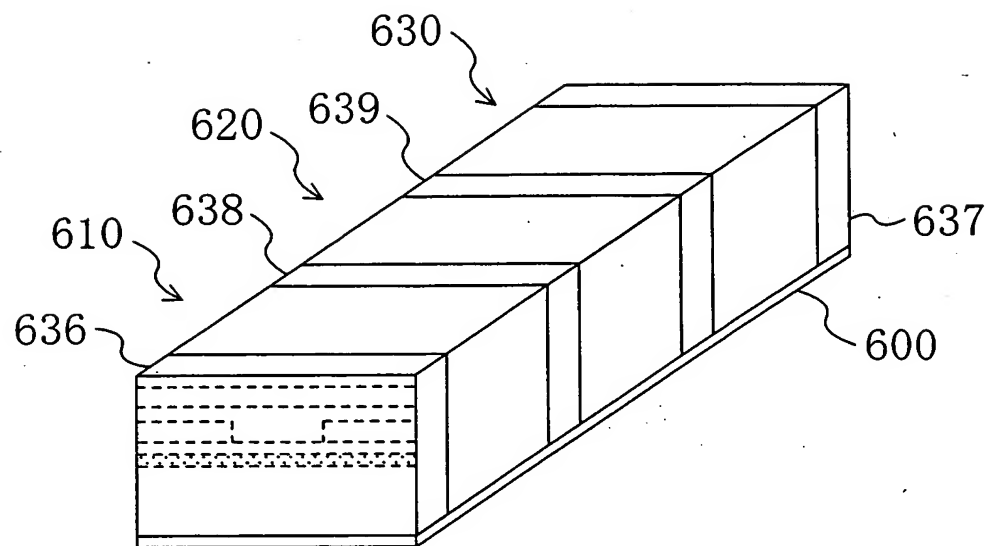


FIG. 21
PRIOR ART

